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TC 2800 MAIL ROOM

REMARKS

Claims 1-8 were pending in the application at the time of this office action. Claims 1, 4, and 8 have been amended. Claims 9 and 10 have been added. Thus, claims 1-10 are present for examination. Re-examination and reconsideration of the application in view of the following remarks are requested.

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art in view of Watt, U.S. Patent No. 5,701,024. The examiner correctly notes that applicant's admitted prior art does not teach a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer. The examiner states, however, that Watt teaches in figure 5 a first conductive type well 54 under a first diffusion layer 44, having a lower dopant concentration than the first diffusion layer.

Independent claims 1, 4, and 8 have been amended. Amended claims 1, 4, and 8 recite, among other features, that the first diffusion layer is not connected to an input/output terminal section. Applicant previously argued at page 5 of the Amendment and Request for Reconsideration dated December 18, 2001, that the prior art of record does not teach each of the claim limitations. While applicant teaches that the first diffusion layer should never be connected to an input/output terminal section, Watt discloses connecting an input terminal 7 to a first diffusion layer 3c. The examiner rejected applicant's argument, at page 8 of the office action, because these features were not recited explicitly in the rejected claims. Thus, applicant has added these features to independent claims 1, 4, and 8.

Thus, amended claims 1, 4, and 8 recite features that are neither disclosed nor suggested in the prior art of record. Watt teaches a first conductive type well 54 under a first diffusion layer 44, in which the first diffusion layer 44 is connected to an input terminal via contact 68. Thus, the prior art of record does not disclose or suggest a first diffusion layer, under which a first conductive type well is formed, wherein the first diffusion layer is not connected to an input/output terminal section. To establish a *prima facie* case of obviousness, each of the claim limitations must be taught or suggested by the prior art of record. In re Royka, 490 F.2d 981,

180 U.S.P.Q. 580 (CCPA 1974). Thus, applicant believes that the PTO cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 with respect to amended claims 1, 4, and 8. Accordingly, claims 1, 4, and 8 are now in condition for allowance.

Claims 2, 3, 5-7, 9, and 10 are each dependent, directly or indirectly, on claims 1, 4, or 8. Thus, applicant believes that these claims are likewise in condition for allowance.

Moreover, there is no suggestion or motivation in the prior art of record to combine the references. The examiner stated that it would have been obvious to combine the references in order to reduce contact spiking during ESD events. [Office action, pages 3, 4, 5, 6, 7, and 8.] As discussed above, independent claims 1, 4, and 8 have been amended to recite, among other features, that the first diffusion layer is not connected to an input/output terminal section. Thus, the examiner's stated motivation to combine the references is no longer applicable. In embodiments of applicant's invention, there is no concern about contact spiking in or about the first diffusion layer because the first diffusion layer is not connected to an input terminal. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation to modify the reference or to combine reference teachings. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q. 2d 1438 (Fed. Cir. 1991). Applicant believes that the PTO cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 with respect to claims 1, 4, and 8, as amended, because there is no such suggestion or motivation. Thus, applicant believes that the amendments to claims 1, 4, and 8 will overcome the examiner's rejection under 35 U.S.C. § 103.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art in view of Yamamoto, U.S. Patent No. 5,898,206 or Morihisa, JP 10-173070. Yamamoto teaches, in Figure 10a, a first conductive type well 21 under the first diffusion layer (n+ source region) 3A, and at least partially under an element isolation film 12A, having a lower dopant concentration than the first diffusion layer 3A. In addition, Yamamoto teaches in Figure 10a the essential structure to their device that a first conductive type well (n-type well) 8B is formed under the second diffusion layer (n+ drain region) 3B. Also, an element isolation film 12B is formed to separate a channel region under gate

insulation film 5A from the second diffusion layer (n+ drain region) 3B. This essential structure results in parasitic resistance 20 of N-well 8B as shown in Figure 4. Thus, the essential structure of Yamamoto is quite distinct from the device structure of the present invention.

Moreover, Watt teaches, in Figure 5, a first conductive type well (N-well) 54 under a first diffusion layer (n+ drain region) 44, in which the first diffusion layer (n+ drain region) 44 is connected to an input terminal Vpad (input pad 14) via contact 68.

Applicant teaches, on the other hand, that the first conductive type well (N-well) 1a is formed under a first diffusion layer (n+ source region) 3c. This feature further distinguishes the present invention from Yamamoto and Watt. Thus, the examiner's rejection of claim 8 is respectfully traversed.

Claims 9 and 10 have been added. Applicant believes that claims 9 and 10 are further distinguished from the prior art of record.

Applicant proposed corrections to the drawings in the December 18, 2001, Amendment and Request for Reconsideration in response to the examiner's objections. Applicant hereby requests that the examiner approve the changes.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Re-examination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

Date: June 13, 2002

By _____ 26,495

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TC 2800 MAIL ROOM

Applicant: Yasuyuki MORISHITA

Title: SEMICONDUCTOR DEVICE

Appl. No.: 09/621,614

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Examiner: Nadav, Ori

Art Unit: 2811

MARKED-UP COPY OF AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Sir:

In reply to the Office Action dated March 14, 2002, please amend the above-identified application as follows:

In the Claims:

1. (Twice Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first diffusion layer of a first conductive type and a second diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors;

wherein said dopant diffusion region is connected to a reference potential, and wherein the second diffusion layer is connected to an input/output terminal section;~~ and~~

wherein under the first diffusion layer, there is formed a first conductive

type well with a lower dopant concentration than the first diffusion layer~~.~~; and

wherein the first diffusion layer is not connected to an input/output terminal section.

4. (Twice Amended) A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section that contains a complementary field effect transistor, wherein:

said complementary field effect transistor comprises a first field effect transistor having a first diffusion layer of first conductive type, a second diffusion layer of first conductive type, and a gate electrode that is disposed between these layers and a second field effect transistor having a third diffusion layer of second conductive type, a fourth diffusion layer of second conductive type, and a gate electrode that is disposed between these layers;

wherein a first dopant diffusion region of second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of first conductive type is set at a distance from said second field effect transistor;

wherein the first dopant diffusion region is connected to a first reference potential, the second dopant diffusion region is connected to a second reference potential, and the second diffusion layer and the fourth diffusion layer are each connected to an input/output terminal section~~; and~~

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer~~.~~; and

wherein the first diffusion layer is not connected to an input/output terminal section.

8. (Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first diffusion layer of a first conductive type and a second diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors;

wherein said dopant diffusion region is connected to a reference potential, and wherein the second diffusion layer is connected to an input/output terminal section;

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer; ~~and~~

wherein the first conductive type well at least partially underlies an element isolation film~~.~~; and

wherein the first diffusion layer is not connected to an input/output terminal section.